REMARKS

In response to the Final Office Action dated February 5, 2009, Applicant requests reconsideration based on the amendments herein and at least the following remarks. Applicant respectfully submits that the claims as presented herein are in condition for allowance.

Claims 1-39 are pending in the present application. Claims 1, 8, 11, 15, 26 and 28 have been amended, while claim 27 is herein canceled, leaving claims 1-26 and 28-39 remaining for consideration.

No new matter has been added by the amendments; rather the amendments herein have been made to incorporate subject matter from allowable dependent claims into corresponding independent claims, as described in further detail below. Accordingly, support for the amendments to claims 1, 11 and 26 can be found in claims 8, 15 and 27, respectively, as originally filed. In addition, claim 8,15 and 27 have been amended in light of the respective amendments to claims 1, 11 and 26, while claim 28 has been amended to change dependency from claim 27 (now canceled) to claim 26.

Applicant respectfully requests reconsideration of claims 1-26 and 28-39 based upon the amendments and at least the following remarks.

Claim Amendments

The Amendments here presented are made for the purposes of better defining the invention, rather than to overcome the rejections for patentability. No presumption should therefore attach that the claims have been narrowed over those earlier presented, or that subject matter or equivalents thereof to which the Applicant is entitled has been surrendered.

Claim Rejections Under 35 U.S.C. §102

To anticipate a claim under 35 U.S.C. § 102, a single source must contain all of the elements of the claim. *Lewmar Marine Inc. v. Barient, Inc.*, 827 F.2d 744, 747, 3 U.S.P.Q.2d 1766, 1768 (Fed. Cir. 1987), cert. denied, 484 U.S. 1007 (1988). Furthermore, the single source must disclose all of the claimed elements "***arranged as in the claim***." Structural Rubber Prods. Co. v. Park Rubber Co., 749 F.2d 707, 716, 223 U.S.P.Q. 1264, 1271 (Fed. Cir. 1984) (Emphasis added).

Claims 1-4, 7, 10-12, 22, 26 and 36 stand rejected under 35 U.S.C. § 102(e) as being allegedly unpatentable over Park, et al. (U.S. Patent No. 7,185,295, hereinafter "Park") as stated on pages 2-7 of the Final Office Action. Applicant respectfully traverses for at least the following reasons.

With respect to independent claim 1, Applicant respectfully notes that a portion of the subject matter of allowable dependent claim 8 has been amended into claim 1. Specifically, claim 1 now recites, *inter alia*, "output data…which comprises a system clock count value of a chip design verification program when the output value of the software block is changed" which Applicant respectfully submits is neither taught nor suggested by Park.

In addition, Applicant notes that Park discloses, primarily in FIGS. 2 & 16a to 16c and columns 20 and 21, that data are continuously transmitted from the interface means 32 of the computer mainframe 2 to the target 34 and/or from the target 34 to the interface means 32. Put another way, the interface means of Park always inputs or outputs all of the data. More specifically, for example, as shown in FIGS. 16a to 16c, data S2T, indicated by dotted areas, is continually and wholly transmitted from the interface means 32 to the target 34 and vice versa. (See, e.g., the second interval, shown in FIG. 16a and described at column 20 lines 26-34.)

Accordingly, Applicant respectfully disagrees with the assertion on page 3 of the Office Action that, since valid data, supplied from the interface means, is kept when consistent with expected data (steps 360 and 370 of FIG. 15a), this discloses the

limitations of applying only valid output data of the software block to the hardware block, via the interface means, and applying only valid output data of the at least one hardware block to the at least one software block (also via the interface means) as the abovementioned steps of Park merely direct that, when data (already inputted from the interface means) are inconsistent, the CPU goes back to find a starting point of a mismatch data to recover the data (step 380). Thus, the interface means of Park is constantly inputting/outputting all data.

Thus, in contrast and in accordance with the present invention, as specifically recited in claim 1 and shown at least in FIG. 3 and described in paragraphs [0028], [0064] and [0069] of the published instant application, the interface means 220 applies only the valid output data of the software block (211, 212, 213, 214 of FIG. 3) to the hardware block 200, and the controller applies only the valid output data of the hardware block 200 to the software block (211, 212, 213, 214) (via the interface means 220).

Thus, the interface means of the present application determines whether the output data of the software block (which includes a system clock count value of a chip design verification program when the output value of the software block is changed) is valid, and applies only the valid output data of the software block to the hardware block. Likewise, the controller of the present invention determines whether the output data of the hardware block (input via the interface means) is valid, and applies only the valid output data of the hardware block to the software block. As a result, the chip design verification apparatus of the present application applies only the valid output data of the software block to the hardware block, and applies only the valid output data of the hardware block to the software block. Put another way, the interface means of the present invention does not continuously input or output all of the data, as is the case in Park.

Therefore, Park does not teach or suggest "an interface means of transmitting output data of the hardware block, [the interface means] determining whether output data of the software block which comprises a system clock count value of a chip design verification program when the output value of the software block is changed is

valid, and [the interface means] applying only valid output data of the software block to the hardware block…transmitting the output data of the software block generated by an operation of executing the chip design verification program to the interface means…determining whether the output data of the at least one hardware block input via the interface means is valid, and applying only valid output data of the at least one hardware block to the at least one software block [via the interface means]" as in independent claim 1. As a result, Park does not disclose all of the claimed elements arranged as in claim 1.

Thus, it is respectfully submitted that claim 1, including claims depending therefrom, i.e., claims 2-10, define over Park.

Accordingly, it is respectfully requested that the above rejection to claims 1-4, 7 and 10 under 35 U.S.C. § 102(e) be withdrawn.

In addition regarding dependent claim 4, Applicant respectfully disagrees that Park discloses the interface means generates "multi clocks," as in the present invention (see, e.g., FIG. 7B, illustrating that the "multi clocks" of claim 4 are separate and distinct first through N-th target clocks). However, referring to column 7, lines 59-62 and column 18, lines 12-21 of Park, as cited by the Examiner on page 6 of the Office Action, Park discloses only that "the clock controller receives clock signals from the PCI bus, the external clock generator, the target, and so on to generate internal and external clock signals of the interface means 32" and "the interface means 32 stop inputting the clock signals applied to the target 34 from the clock controller 66…[and] an input of the clock signals applied from the clock controller 64 of the interface means 32 to the target 34 is stopped," which provide no indication that separate and distinct, e.g., multi, clock signals are utilized in Park.

Thus, it is respectfully submitted that claim 4, including claims depending therefrom, i.e., claims 5 and 6, define over Park for this additional reason as well.

Accordingly, it is respectfully requested that the above rejection to claim 4 under 35 U.S.C. § 102(e) be withdrawn for this additional reason, as well.

With respect to independent claim 11, Applicant respectfully notes that, similar as to discussed above with respect to claim 1, a portion of the subject matter of allowable dependent claim 15 has been amended into claim 11. Specifically, claim 11 now recites, *inter alia*, "output data…which comprises a system clock count value of the chip design verification program when the output value of the software block is changed" which Applicant submits is neither taught nor suggested by Park.

Also similar to as discussed above, Applicant respectfully submits that Park teaches that valid data, continuously inputted/outputted from the interface means, is kept when consistent with expected data (steps 360 and 370 of FIG. 15a) but, regardless, the interface means of Park always inputs or outputs all of the data.

In contrast and in accordance with the present invention, as specifically recited in claim 11 and described in greater detail above with respect to claim 1, the interface means of the present application determines whether the output data of the software block (which includes a system clock count value of a chip design verification program when the output value of the software block is changed) is valid, and applies only the valid output data of the software block to the hardware block. Likewise, only the valid output data of the hardware block is applied to the software block (via the interface means).

Therefore, Park does not teach or suggest "…a software side operation step of transmitting output data generated by the operation of the software block to the interface means, determining whether the output data of the hardware block which comprises a system clock count value of the chip design verification program when the output value of the software block is changed received via the interface means is valid by executing the chip design verification program, and applying only the valid output data of the hardware block to the software block [via the interface means]…determining whether the output data of the software block received is valid by executing the chip design verification program in the interface means, and applying only the valid output data of the software block to the hardware block [via the interface means]" as in independent claim 11. As a result, Park does not disclose all of the claimed elements arranged as in claim 11.

Thus, it is respectfully submitted that claim 11, including claims depending therefrom, i.e., claims 12-25, define over Park.

Accordingly, it is respectfully requested that the above rejection to claims 11-12 and 22 under 35 U.S.C. § 102(e) be withdrawn.

In addition regarding dependent claim 12, Applicant respectfully disagrees that Park discloses the interface means generates multi clocks, as in the present invention, as discussed above with respect to claim 4.

Thus, it is respectfully submitted that claim 12, including claims depending therefrom, i.e., claims 13-25, define over Park for this additional reason as well.

Accordingly, it is respectfully requested that the above rejection to claim 12 and 22 under 35 U.S.C. § 102(e) be withdrawn for this additional reason, as well.

With respect to independent claim 26, Applicant respectfully notes that the subject matter of claim 27 in its entirety, which the Examiner states on page 7 of the Office Action is allowable, has been amended into claim 26.

Therefore, Park does not teach or suggest "wherein the output data of the hardware block has an output value of the hardware block changed in response to the multi clocks applied from the interface means, and a system clock count value of the interface means when the output value of the hardware block is changed" as in independent claim 26. As a result, Park does not disclose all of the claimed elements arranged as in claim 26.

Thus, it is respectfully submitted that claim 26, including claims depending therefrom, i.e., claims 28-39, define over Park.

Accordingly, it is respectfully requested that the above rejection to claims 26 and 36 under 35 U.S.C. § 102(e) be withdrawn.

Allowable subject matter

Claims 5, 6, 8, 9, 13-21, 23-25, 27-35 and 37-39 are objected to as being dependent on rejected base claims, but would be allowable if rewritten in independent

form to include all of the limitations of the base claims and any intervening claims, as stated on pages 7-8 of the Final Office Action.

Regarding claim 27, Applicant gratefully acknowledges the Examiner's noting the allowable subject matter therein, and respectfully notes, as discussed above, that the allowable subject matter has been incorporated into independent claim 26, from which claim 27 (now canceled) depended.

Regarding the remaining claims, i.e., claims 5, 6, 8, 9, 13-21, 23-25, 28-35 and 37-39, Applicant gratefully acknowledges the Examiner's noting the allowable subject matter in the abovementioned claims, and notes that some subject matter from claims 8 and 15 has been amended into independent claims 1 and 11, respectively, but Applicant further respectfully notes that claims 5, 6, 8, 9, 13-21, 23-25, 28-35 and 37-39 are allowable as depending upon allowable independent claims 1 and 11, as discussed above. As such, Applicant has not rewritten claims 5, 6, 8, 9, 13-21, 23-25, 28-35 and 37-39 in independent form at this time.

Conclusion

In view of the foregoing remarks distinguishing the prior art of record, Applicant respectfully submits that this application is in condition for allowance. Early notification to this effect is requested. The Examiner is invited to contact Applicant's attorneys at the below-listed telephone number regarding this Amendment or otherwise regarding the present application in order to address any questions or remaining issues concerning the same. If there are any charges due in connection with this response, including for any required extension(s) of time, for which the Applicant hereby respectfully petitions, please charge them to Deposit Account 06-1130.

Respectfully submitted,

CANTOR COLBURN LLP

By: /Noah J. Hayward/
James J. Merrick
Registration No. 43,801
Noah J. Hayward
Registration No. 59,515
Cantor Colburn LLP
1800 Diagonal Rd, Ste 510
Alexandria, VA 22314
Telephone (703) 236-4500
Customer No. 23413

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